

REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested. Claims 1-4, 6-11, 13, 16, and 17 (total number of claims 13) remain pending in the present application. Claims 1 and 7 are independent claims.

Objections

In the recent Office action, the Examiner objected to the Drawings. In particular, the Examiner objected to Figs. 9 and 10 because they illustrate Prior Art without being designated as such. A proposed Drawing Change Authorization Request is submitted herewith. Proposed changes are shown in red. Specifically, Figs. 9 and 10 have been designated by the legend --Prior Art--. Therefore, the Examiner's objection with respect to the Drawings is overcome.

The Examiner objected to the Specification because of various informalities. Applicant has corrected the various informalities by amending the Specification as shown above, and the objection with respect to the Specification is overcome.

Rejections Under 35 U.S.C. § 112

The Examiner rejected claim 5 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has incorporated the subject matter of claim 5 into claim 1, and accordingly Applicant has cancelled claim 5. Therefore, the rejection with respect to claim 5 is rendered moot.

**Rejections Under 35 U.S.C. § 102**

The Examiner rejected claims 1-4 and 7-11 under 35 U.S.C. § 102(e) as being anticipated by Ma et al., U.S. Patent No. 5,939,753, hereafter “Ma”. The Examiner asserts that Ma shows all of the elements recited in claims 1-4 and 7-11. Applicant submits that Ma fails to disclose a semiconductor device with a first interconnection connected to a gate of the MOSFET, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET; a high concentration impurity diffused region located under the first interconnection and at a surface part of the semiconductor substrate; a second interconnection connected to the high concentration impurity diffused region; and a low resistance layer provided on the upper surface of the high concentration impurity diffused region, as recited in claims 1 and 7.

Ma discloses, for example, in Fig. 8, that the first interconnection 133 connects to a gate 55 and the second interconnection 135 connects between one electrode of the DPC (double polysilicon capacitor) 89 and the highly concentrated impurity diffused region 89 (substrate). At col. 8, lines 21-22, Ma discloses that the metallization region 133 (first interconnection) is electrically coupled to gate electrode 105. With respect to the Examiner’s contention that elements 135, 89, and 99 of Ma meet Applicant’s claimed features, this is in error. Elements 135, 89, and 99 are disclosed as portions of the DPC 57, not the IGFET 115.

Therefore, Ma does not disclose the claimed semiconductor device with the following spatial relations as recited in claims 1 and 7 (and claims 2-4, 6, 8-11, 13, 16, and 17 by virtue of dependency): the first interconnection 115, which constitutes a signal input pad 116 for receiving an input signal, is connected to a gate 107 of the MOSFET; the high concentration impurity diffused region 112 is disposed under the

first interconnection 115; the second interconnection 117 is connected to the high concentration impurity diffused region 121; the gate 107 and the high concentration impurity region 121 are not connected because their functions are different. The features of the present invention provide the high concentration impurity diffused region for eliminating any substrate potential. This region is disposed beneath the signal input interconnection, and is connected to the gate of the MOSFET device.

Applicant respectfully submits that claims 1 and 7 (and claims 2-4, 6, 8-11, 13, 16, and 17 by virtue of dependency) are not anticipated by Ma, and are allowable.

**Rejections Under 35 U.S.C. § 103**

The Examiner rejected claims 5 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Ma as applied to claims 1-4 and 7-11 above, and further in view of Muira, U.S. Patent No. 5,932,917. Applicant has incorporated subject matter from claims 5 and 12 into claims 1 and 7 respectively, and accordingly Applicant has cancelled claims 5 and 12. Therefore, the rejection as applied to claims 5 and 12 is rendered moot. With respect to the rejection being applied to claims 1 and 7, Applicant submits that claims 1 and 7 are not anticipated by Ma. In particular, claims 1 and 7 are patentable over Ma as discussed above with respect to the arguments presented to overcome the 35 U.S.C. § 102(e) rejection.

The Examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Ma as applied to claims 1-4 and 7-11 above, and further in view of Morifushi, U.S. Patent No. 5,990,504, issued November 23, 1999. It is noted that the present application has a priority date of January 29, 1999, which is prior to the patent date of Morifushi. Therefore, the application of the Morifushi reference is improper and should be withdrawn. Thus, this particular ground of rejection is moot. Applicant

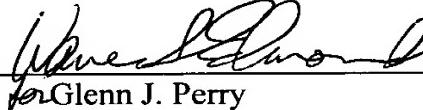
respectfully requests that the rejection of claims 6 and 13 be withdrawn and these claim allowed.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned "Version with markings to show changes made".

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,  
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Enclosure: Appendix

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification has been changed as follows:

Page 3, the whole paragraph starting in line 18 has been deleted and replaced with the following new paragraph:

The semiconductor device according to the present invention includes the low-resistance layer provided under the interconnection extending from the [singal] signal input, whereby the substrate resistance is decreased by this low-resistance layer, the heat noises caused by the substrate resistance can be reduced, and the noise characteristic of the semiconductor device can also be improved.

Page 3, the whole paragraph starting in line 18 has been deleted and replaced with the following new paragraph:

Next, a gate oxide layer 123 is provided in the device region by thermal oxidation, polysilicon is deposited thereon, and patterning is effected thereon, thereby obtaining a gate electrode 107 (FIG. 4). In an example shown in FIG. 4, the gate electrode and an impurity diffused region peripheral to this gate electrode take a well-known LDD structure. To be specific, after providing the gate electrode 107, with the gate electrode serving as an ion implantation mask, ions are implanted into the device region by a comparatively low energy, whereby a low-concentration diffused layer 131 is formed shallow. Subsequently, insulating layers such as silicon nitride layer and silicon oxide layer are deposited on the whole and etched back by an anisotropic